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Engineering Note

Date: December 7, 2001
Rev Date: December 19, 2001

Project: CFT / AFE
Doc. No: A1011207

Subject: Details of upgrades to AFE Bulk Power Supply Firmware (Version 7)

Introduction

In the weeks following installation of significant numbers of AFE boards to the detector an unacceptably large number of power supply trip conditions have been reported. A 'search and measure' expedition during one access indicates that there are no grounding or short circuit problems. Analysis of the state machine logic implemented on the power supply monitor board shows a number of flaws. To correct these flaws new firmware has been created. This note describes the new firmware, fully defines the physical interconnections and explicitly defines the communication protocol which must be used.

Firmware Overview

This version (Version #7.2) replaces the Version 6.0 code installed in the platform. The firmware is implemented as a pair of state machines which respond to control signals from an external Rack Monitor and to undervoltage (trip) conditions sensed by local comparators (overvoltage is internally sensed by the Vicor). In response to control signals the firmware enables or disables the individual DC-DC converters in a Vicor power supply box. Errors result in the state machine entering fault-trap states which hold the supplies in the disabled mode until the fault is reset by external software.

The Altera files for the CPLD are located at

D0SERVER4.fnal.gov/projects/triggerelectronics/CAE/AFE power supply/V7.2_Firmware

and were last compiled using Altera version 9.6. A MAX7128LC84 is used.

Control of the State Machines via Rack Monitor Software

Each AFE Bulk Power Supply is connected to one Digital Output cable of a Rack Monitor which delivers sixteen control bits. Two identical state machines (one for each backplane connected to the Power Supply) exist. Each supply has two control bits (*request turn on* and *request turn off*). There is also one *global reset* which resets one or both machines dependent upon the settings of the control bits.

- Bit 3 is the *request turn on* bit for the 'A'[1] backplane. Bit 5 is the *request turn off* bit for the 'A' backplane.
- Bit 7 is the *request turn on* bit for the 'B' backplane. Bit 9 is the *request turn off* bit for the 'B' backplane.
- Bit 1 is the *global reset* bit. A logic high on this bit whenever both of the *request* bits for a backplane are high, or both are low, requests that the state machine for that backplane be reset to its power-up state. The *global reset* bit is *inactive* in either of the usual operational states.

[1] The 'A' backplane is the one to the left of the viewer when looking at the crate from the front.

The two bits for a backplane are coupled to each other, and to the global reset bit, in order to minimize spurious transitions. The eight combinations of these bits are summarized in Table 1. Each backplane *operates independently following the rules of Table 1*. Only those states in which one and only one bit is set of the three, or when all three are set, can cause a change of state[2]. Multiple bit transitions in opposite directions are required to change from one action to another, minimizing the chances of random noise causing an unplanned state transition. Having two different definitions of the reset condition is supplied so that if the *request turn on* bit is shorted to VCC, or the *request turn off* bit is shorted to GND, the supplies can still be remotely turned off. The other short conditions are inherently safe, since they force the supplies off.

Request OFF	*Reset*	*Request ON*	State Machine Response
0	0	1	State machine turns supplies on if they are off, but *not* if any trip or error condition is present.
0	1	0	State machine is re-set to power-up condition (supplies off)
1	0	0	State machine turns supplies off if they are on; also acknowledges any trip/error condition and re-enables supplies to be turned on again.
1	1	1	State machine is re-set to power-up condition (supplies off)
0	0	0	State does not change.
1	0	1	State does not change.
0	1	1	State does not change.
1	1	0	State does not change.

Table 1

Correct Algorithm to Use the AFE Power Supplies

The coding mechanism of the state machine is optimized for Grey Code transitions in the control bits. Using Grey coded transitions *requires that two writes be performed to the Rack Monitor for any requested change of state.* Always use two writes, changing only one bit at a time, to minimize crosstalk between control cables and system noise. *Do not use pulses, set bits and leave them set until a new state transition is necessary.* Remember when reading these steps that the two halves of the power supply are independent and have independent control bits.

- To turn the power supplies ON:
  - Write a word to the digital output latch of the Rack Monitor which has *request_on*, *request_off* and *reset* all off.
  - Write a word to the digital output latch of the Rack Monitor which has *request_on* set and other bits clear.
  - Read the digital status word from the digital input latch of the Rack Monitor to verify all supplies turned on. Remember that the SUPPLIES_ON bit is the AND of the two halves, so the bit won't be set unless both are on.
- To turn the power supplies OFF:
  - Write a word to the digital output latch of the Rack Monitor which has *request_on*, *request_off* and *reset* all off.
  - Write a word to the digital output latch of the Rack Monitor which *request_on* set and the other two bit clear, *and leave them that way.*
  - Read the digital status word from the digital input latch of the Rack Monitor to verify all supplies turned off.

[2] Karnaugh map fans will recognize this as the typical 'checkerboard' pattern.

- To sense & recover from a trip condition, failure-to-turn-on condition, etc.:
  - Read the digital status word from the digital input latch of the Rack Monitor to record the status of the supplies.
  - Save the status data into the system logs. Examine the specific system status bits of the word read to identify the general cause of failure, then identify which DC-DC converter(s) are not in the correct state by looking at the specific converter status bits in the status word.
  - The digital control word to the supply as driven by the Rack Monitor should, at this state, have the *request_on* bit set and the *request_off* bit clear, because that's the state it was left in after turning the supply on. To acknowledge the error, one must write two words to the Rack monitor- first, write a word with the *request_on* and *request_off* both clear, then a second word with *request_off* set and *request_on* clear. One may then later re-enable the supply using the normal sequence.
- The controller state machines should never, *ever*, need to be reset unless the control cable has shorts to VCC or GND. However, for those who think they know better, a reset may be accomplished by:
  - Write a word to the digital output latch of the Rack Monitor which has the *request_on* and *request_off* bits both clear.
  - Write a word to the digital output latch of the Rack Monitor which has the *request_on* and *request_off* bits both clear, and the *reset* bit set.
  - This does exactly the same thing and will leave the state machine in exactly the same place as performing the turn off sequence given above. Remove the reset bit and turn on again when desired.

Digital Status and Internal Connections of the Monitor Board

The AFE Bulk Power Supplies provide a sixteen bit digital status word containing state machine and trip information to the Rack Monitor. The PC Board layout of the Monitor Board happens to tie a couple of the Status bits to signal lines which are used in the AFE implementation as control bits, so a short digression is in order. The Monitor Board schematics ,found on the Web at

http://D0server1.fnal.gov/projects/CalorimeterElectronics/WWW/HuffyKnows/schematics/montop.pdf

, show a sixteen bit bus connected between the Rack Monitor interface connector, the internal Altera CPLD and header connector J27. In the AFE implemention, J27 is used as the *output connector* from the PLD to the Vicor power supplies. This usage, although sensible mechanically, means that the signal names in the Monitor Board schematic have little to do with the actual functions of the bits. There is also the unfortunate situation where some bits used as *control* bits from PLD to Vicor get copied into *status* bits because the pins are shorted together on the Monitor Board. A little cut-and-paste from the Monitor Board schematic with some touchup will show the connectivity of interest in Figure 1.

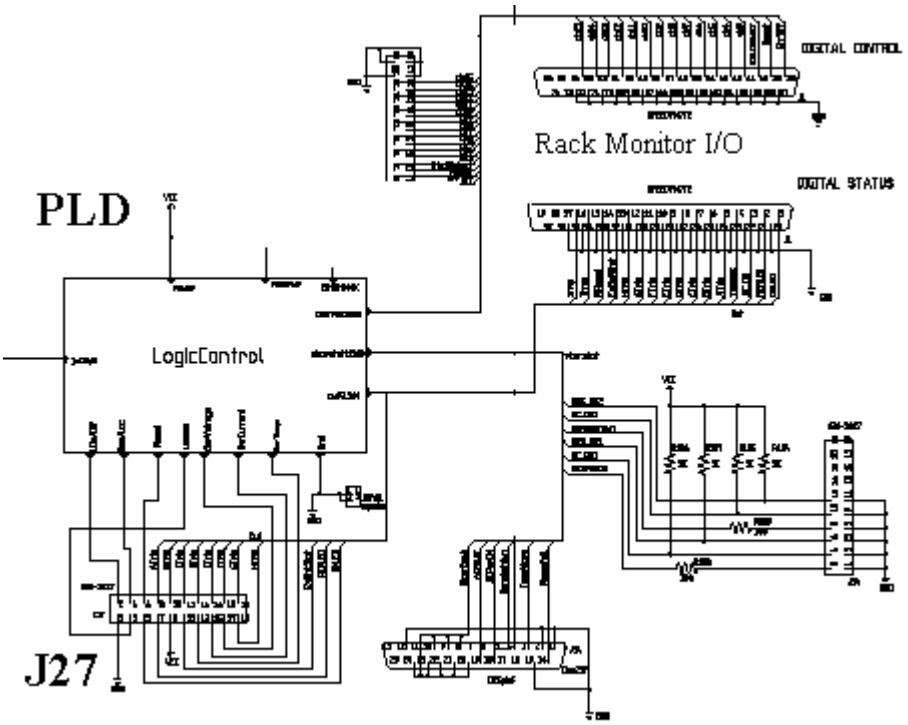

Figure 1

As Figure 1 shows, the Digital Status back to the Rack Monitor is connected to the PLD by a bus which also goes to J27. There are seven lines going to J27 which are not connected to the bus, but 10 lines are required for the interface to the Vicor supplies used with the AFE boards (8 for individual enables, one for AC-OK and one for general shutdown). Thus, three of the Digital Status bits will be connected to control lines and may be meaningless as status bits. This does, however, leave 13 bits available for status. We have chosen to use ten of these to report the sampled status of the ten DC-DC converters and use the other three as general status bits.

Table 2 maps out the Monitor Board signal names to what functions they *really* have in the AFE implementation, and also to what bit they show up as in the digital readback.

READ THIS!

Digital status bits reflecting individual supply status presented to the Rack Monitor are ***latched status bits, not the live-at-the-moment Vicor status.*** The Vicor status bits ***are latched when an error is detected***. The state machines in the PLD will detect the error and turn the supplies off, leaving ***the reason WHY the supplies were turned off*** in the status bits. Do not interpret the individual supply status bits as an indication of a problem in progress. The ***general status bits*** are the bits which tell you whether a problem is present or not. If all three of these bits are OK, the supply is working.

Bit Position in Readback	Status Meaning if Set	Monitor Board Signal Name	J27 Pin on Monitor Board	AFE Vicor Control Usage
15	Trip Error; set if *either* state machine has an error.	Itrip	N/A	N/A
14	Turnon Error; set if *either* state machine has an error.	Vtrip	N/A	N/A
13	Shows copy of enable bit; ignore for status	Mreset	3	Enable +5.5V 'A' from PLD to Vicor
12	Supplies ON; *both backplanes must be on for this bit to be set.*	ExtIntStat	11	N/A
11	–12V 'B' OK	Htrip	19	-12V 'B' pwr OK to PLD
10	+12V 'B' OK	Gtrip	20	+12V 'B' pwr OK to PLD
9	–12V 'A' OK	Ftrip	18	-12V 'A' pwr OK to PLD
8	+12V 'A' OK	Etrip	16	+12V 'A' pwr OK to PLD
7	+5.5V 'B' OK	Dtrip	14	+5.5V 'B' pwr OK to PLD
6	+5.5V 'A' OK	Ctrip	12	+5.5V 'A' pwr OK to PLD
5	+5V 'B' OK	Btrip	10	+5V 'B' pwr OK to PLD
4	+5V 'A' OK	Atrip	8	+5V 'A' pwr OK to PLD
3	+3.3V 'B' OK	TempOK	N/A	+3.3V 'B' pwr OK to PLD
2	+3.3V 'A' OK	AC_OK	N/A	+3.3V 'A' pwr OK to PLD
1	Shows copy of "AC OK" from Vicor	REMLED	7	"AC OK" status from Vicor back to PLD
0	Shows copy of ±12V 'A' enable; ignore for status	ONLED	5	Enable ±12V 'A' from PLD to Vicor
N/A	N/A	Monitor Vcc	9	N/A
N/A	N/A	Monitor GND	1	N/A
N/A	N/A	LOn/Off	2	Enable +5V 'A' from PLD to Vicor
N/A	N/A	Rem/Loc	4	Enable +3.3V 'A' from PLD to Vicor
N/A	N/A	Reset	6	Enable +5V 'B' from PLD to Vicor
N/A	N/A	OvrVoltage	17	Enable ±12V 'B' from PLD to Vicor
N/A	N/A	OvrCurrent	15	Enable +3.3V 'B' from PLD to Vicor
N/A	N/A	OvrTemp	13	Enable +5.5V 'B' from PLD to Vicor

Table 2

Specific Description of Status Bit Latching Algorithm and State Machine

The state machines in the PLD controlling the power supplies monitor the 'power good' outputs of all eight DC-DC converters in the Vicor box as developed by comparators on the Monitor board. The ±12V supplies have individual 'power good' outputs as there are two converter modules, but the shutdown input of the two is common; therefore, the ±12V is treated as a single supply for control purposes. Dual, identical state machines are implemented for the two sets of supplies (one per backplane, the Vicor services two backplanes). Each state machine waits for the two-bit combination of the Turn_on and Turn_off bits from the Rack Monitor before initiating a power-up sequence. When the command is received the supplies are sequenced as required by the AFE. The only difference between the two machines is which control bits from the Rack Monitor are used to initiate state transitions. Algorithmically, they are identical. A state diagram is given in Figure 2 which may assist while reading the following commentary.

The command to turn on the power supplies must persist for 200 milliseconds to be honored. An internal monostable is used which begins its timeout period when the correct bit pattern is seen. The bit pattern is resampled at the end of the 200msec interval and, if still present, is acted upon. The identical 200msec timer is used for each power supply. As each supply is enabled by the state machine, the timer is restarted. At the end of 200msec, if the supply's 'power good' is present, the machine advances, re-latching the new status in the status latch. If not, the status bits are preserved (holding the error condition) and the state machine enters an error state. The machine *will not advance* from the error state until the error is acknowledged by external software, which is accomplished by setting the Turn_on bit to 0 and the Turn_off bit to 1. This 'latch-and-hold' allows the reported failure to persist until seen by monitoring software. Of course, although the *latched error* persists, the *supplies* are all turned off as soon as the error has been latched. A turn-on error is flagged by bit 14 of the status word being set. All turn-on error latch states assert this status bit. Bit 14 is the OR of the turn-on error from either machine.

Once the supplies are all on, the machine waits in the CHK_OFF_GLTCH state. During this state the SUPPLIES_ON bit (bit 12) is set in the status word. This is in case any fault in the PLD or the system might prevent the supplies from being turned off (for instance, the turn-off bit shorted to GND in a cable). Software can check that the SUPPLIES_ON is cleared in response to turning the supply OFF. If the SUPPLIES_ON bit doesn't go away in response to a turn-off request, the PLD didn't honor that request, and a reset should then be attempted. If turn-off doesn't work but reset does, then there is a fault in the cable or the Monitor board. Under normal conditions, if Turn-off = 1 and Turn-on = 0 is asserted continuously, the machine will simply go back to the idle state and turn the supplies off. The 200 msec timer is utilized to insure that the request is real and not cable noise. Once the bit state requesting turn-off is asserted, it must remain asserted until the 200 msec timer expires or the request is ignored.

Please be reminded that the SUPPLIES_ON bit is the AND of the SUPPLIES_ON status of the two state machines. If either machine has its supplies turned off for any reason, SUPPLIES_ON will be zero.

The machine may also exit from the CHK_OFF_GLTCH state if an undervoltage (trip) condition is sensed. The 200 msec timer is again utilized here. Whenever any trip condition of any number of supplies is sensed, the machine enters a loop where the status is monitored continuously. If the perceived trip "recovers" during the 200msec such that everything looks OK again, the machine ignores the trip assuming it was noise. If at the end of 200msec any trip condition is still present the machine samples the status, turns off all supplies and enters a trip-error state. Once in a trip-error state bit 15 (Trip Error) is set in the status word along with the supply status latched prior to turning off all supplies. The trip-error state persists indefinitely until ackowledged by external software via the mechanism of setting the Turn-off bit and also clearing the Turn-on bit. Again, the Trip Error (bit 15) is the OR of the error state from the two machines.

Monostable Considerations

An unfortunate decision in the Monitor Board is that the dual monostable connected to the CPLD is not set up the same on both sides. One monostable is set to 200 msec but the other is only 8 msec. We have taken the decision in V7.1 of the firmware to OR the two machines together for timing purposes and use the single 200msec timer for both. This could result in oversensitivity such that while one machine is responding to command input or trip conditions the shared timing signal could result in the other machine reacting too quickly to a false trip due to noise. If physical access timing permits, in the future we would change resistor/capacitor values to make both monostables 200msec and use one monostable exclusively for each state machine.

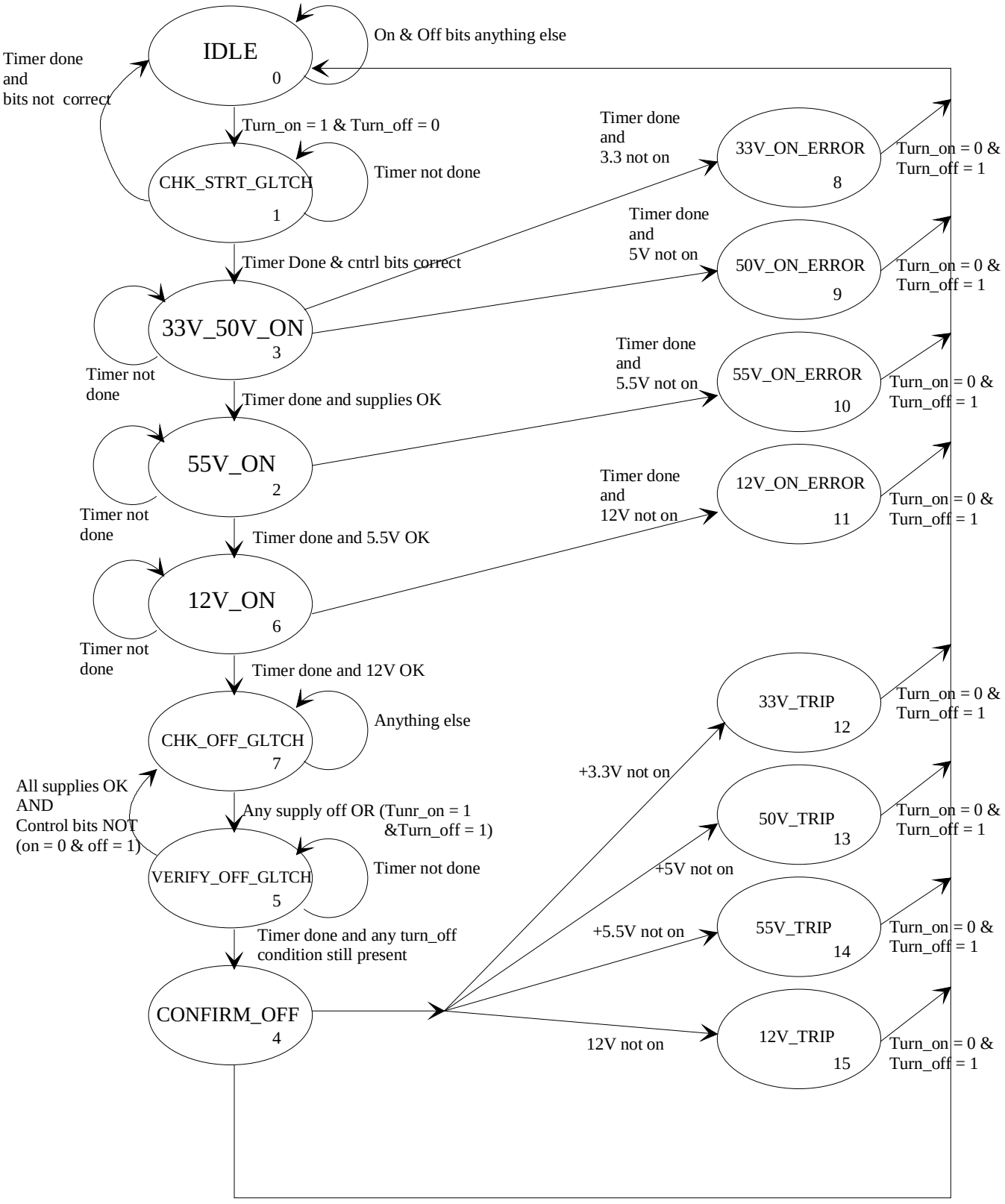
IDLE
0
On & Off bits anything else
Timer done
and
bits not correct
Turn_on = 1 & Turn_off = 0
CHK_STRT_GLTCH
1
Timer not done
Timer Done & cntrl bits correct
33V_50V_ON
3
Timer not
done
Timer done and supplies OK
55V_ON
2
Timer not
done
Timer done and 5.5V OK
12V_ON
6
Timer not
done
Timer done and 12V OK
CHK_OFF_GLTCH
7
Anything else
All supplies OK
AND
Control bits NOT
(on = 0 & off = 1)
Any supply off OR (Tunr_on = 1
&Turn_off = 1)
VERIFY_OFF_GLTCH
5
Timer not done
Timer done and any turn_off
condition still present
CONFIRM_OFF
4
Timer done
and
3.3 not on
33V_ON_ERROR
8
Timer done
and
5V not on
50V_ON_ERROR
9
Timer done
and
5.5V not on
55V_ON_ERROR
10
Timer done
and
12V not on
12V_ON_ERROR
11
+3.3V not on
33V_TRIP
12
+5V not on
50V_TRIP
13
+5.5V not on
55V_TRIP
14
12V not on
12V_TRIP
15
Turn_on = 0 &
Turn_off = 1

Figure 2